

Fig. 1

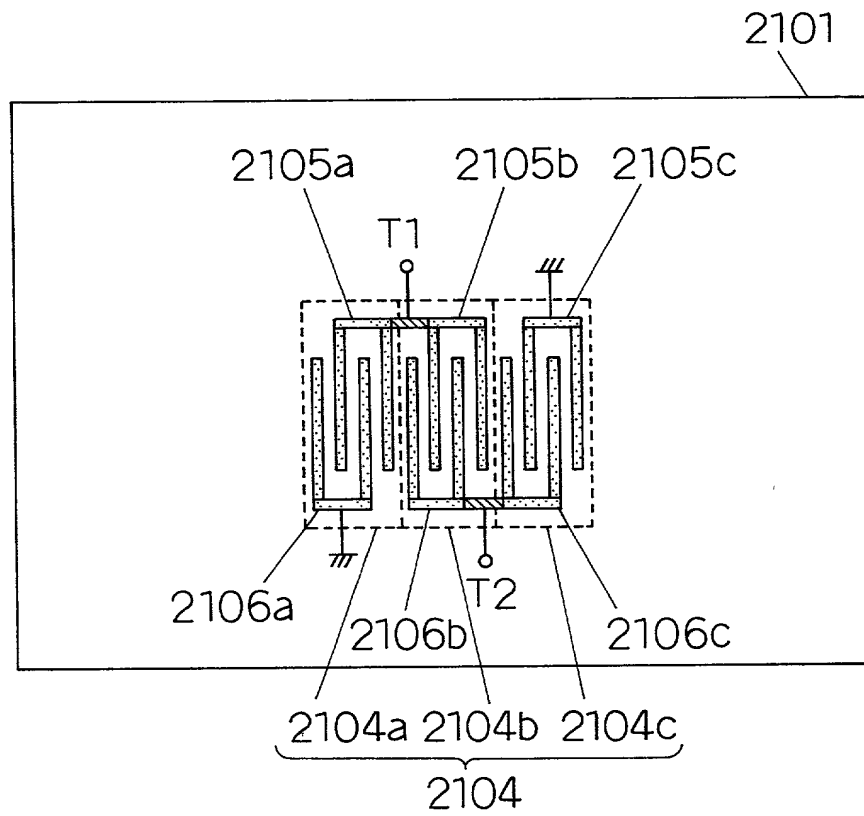


Fig. A1

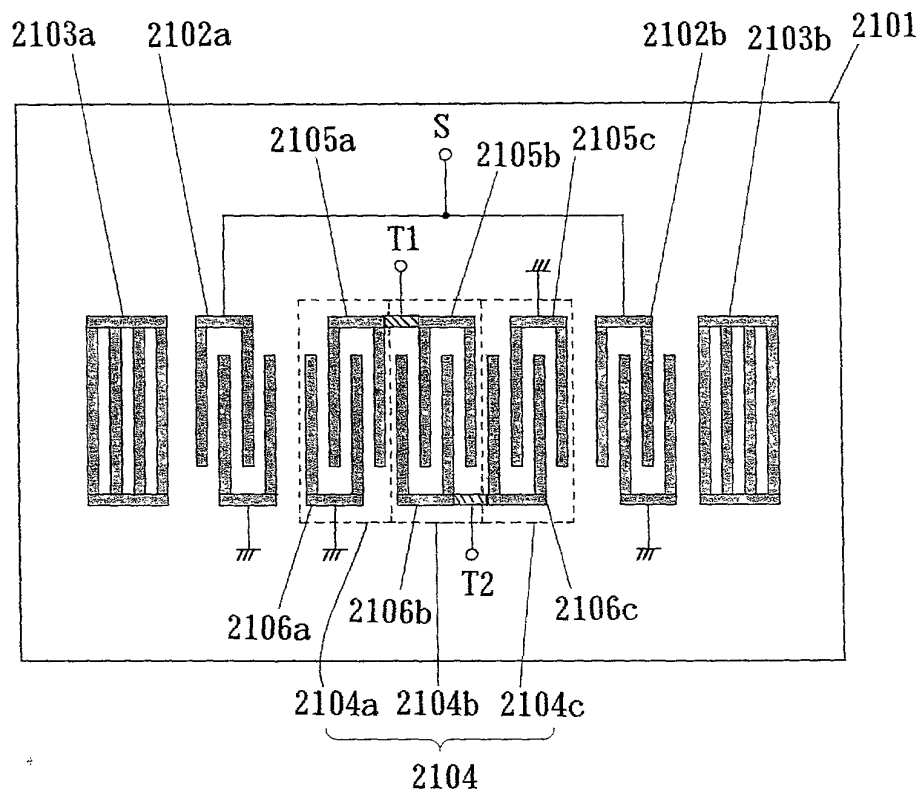


Fig. 2

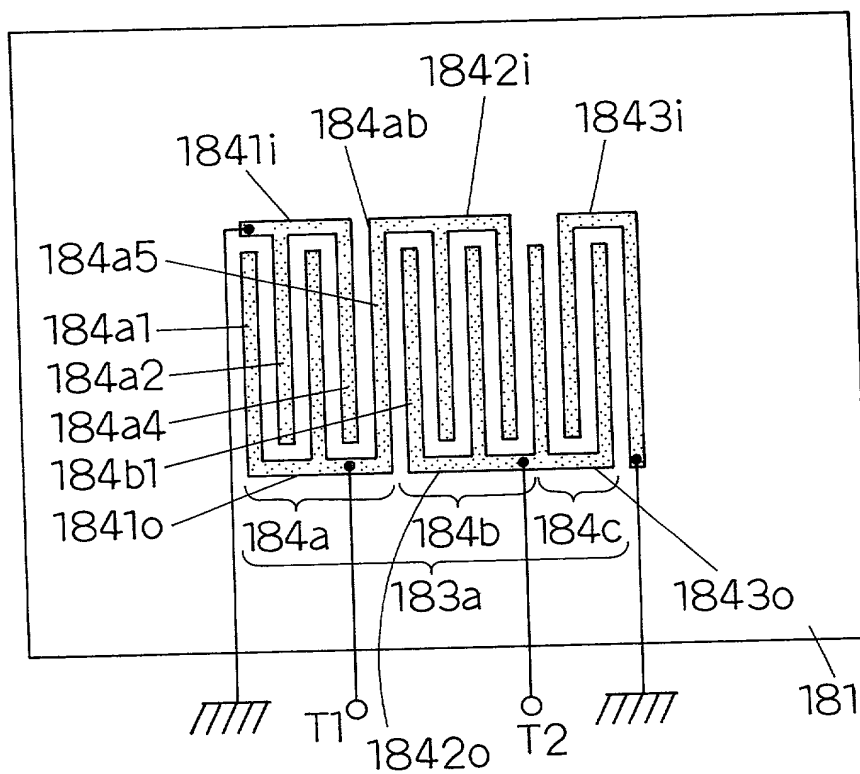


Fig. A2

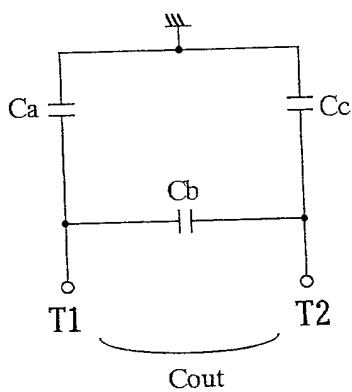


Fig. A3

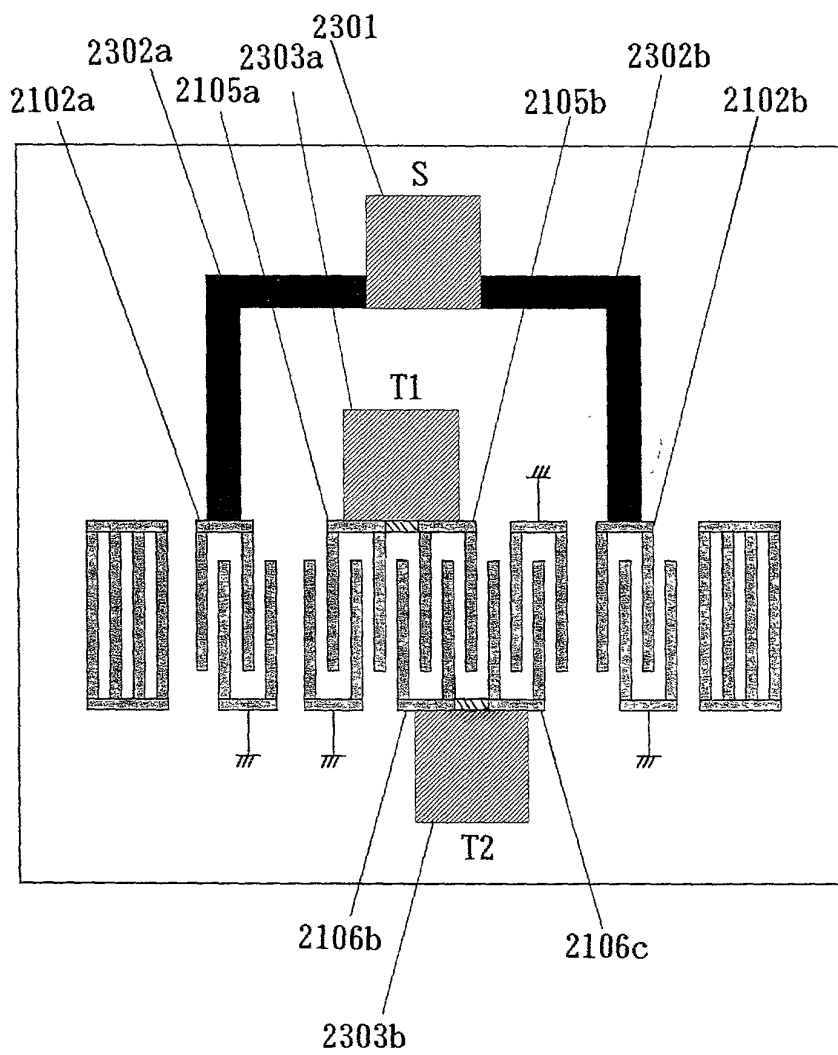


Fig. A4

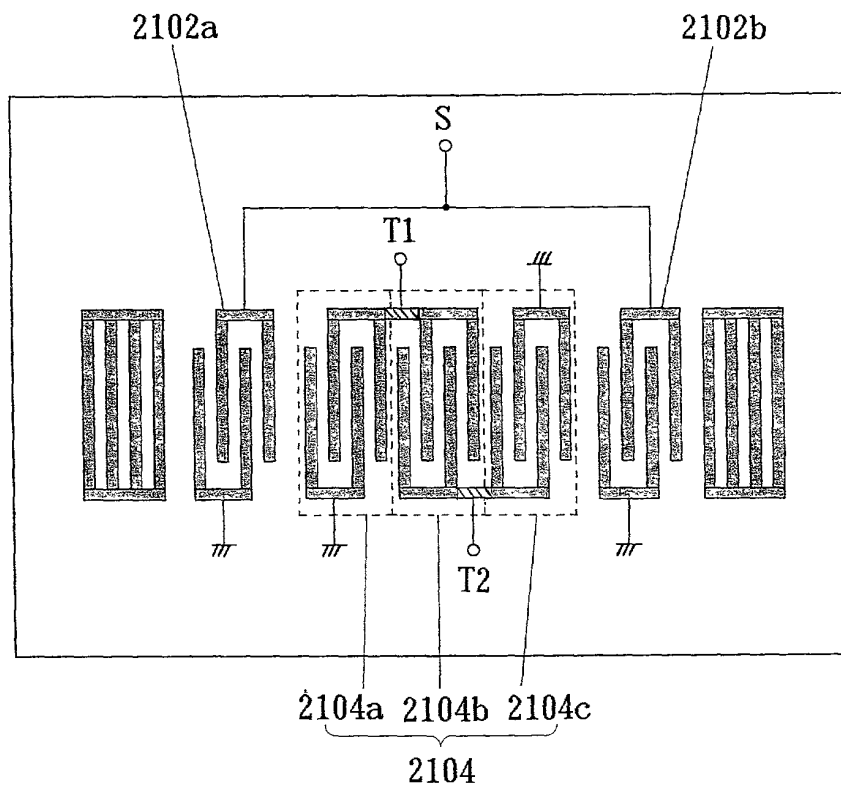
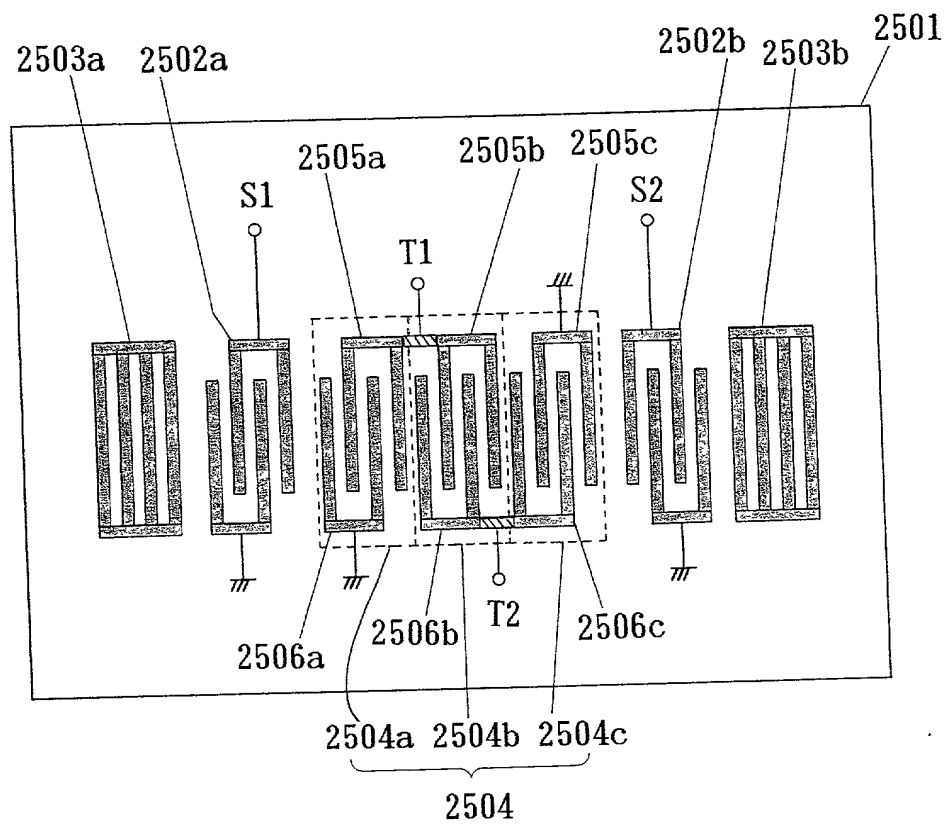


Fig. A5



The diagram illustrates a semiconductor device layout. A central region 2601 is surrounded by various other regions. Regions 2602a, 2602b, and 2603 are located at the top, while 2604, 2605a, 2605b, and 2606 are at the bottom. Regions 2607 and 2608 are on the right side. Regions 2102a, 2102b, 2103a, and 2103b are located on the left side. Regions 2104a, 2104b, and 2104c are located in the center. Regions 2106a, 2106b, and 2106c are located at the bottom. A source region 'S' and a drain region 'T2' are also indicated. The diagram shows a complex arrangement of rectangular and irregular shapes representing different semiconductor layers or regions.



Fig. A7 (a)

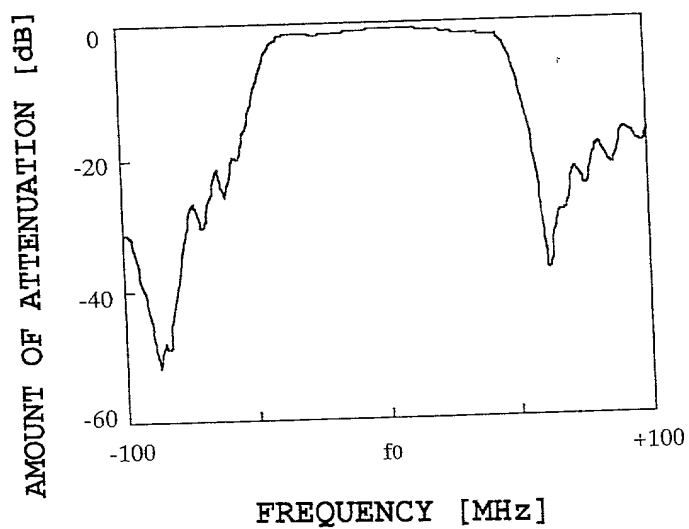


Fig. A7 (b)

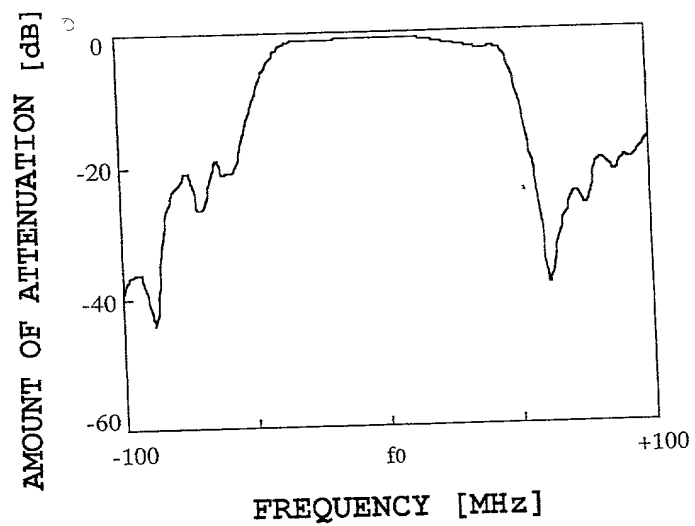


Fig. A8

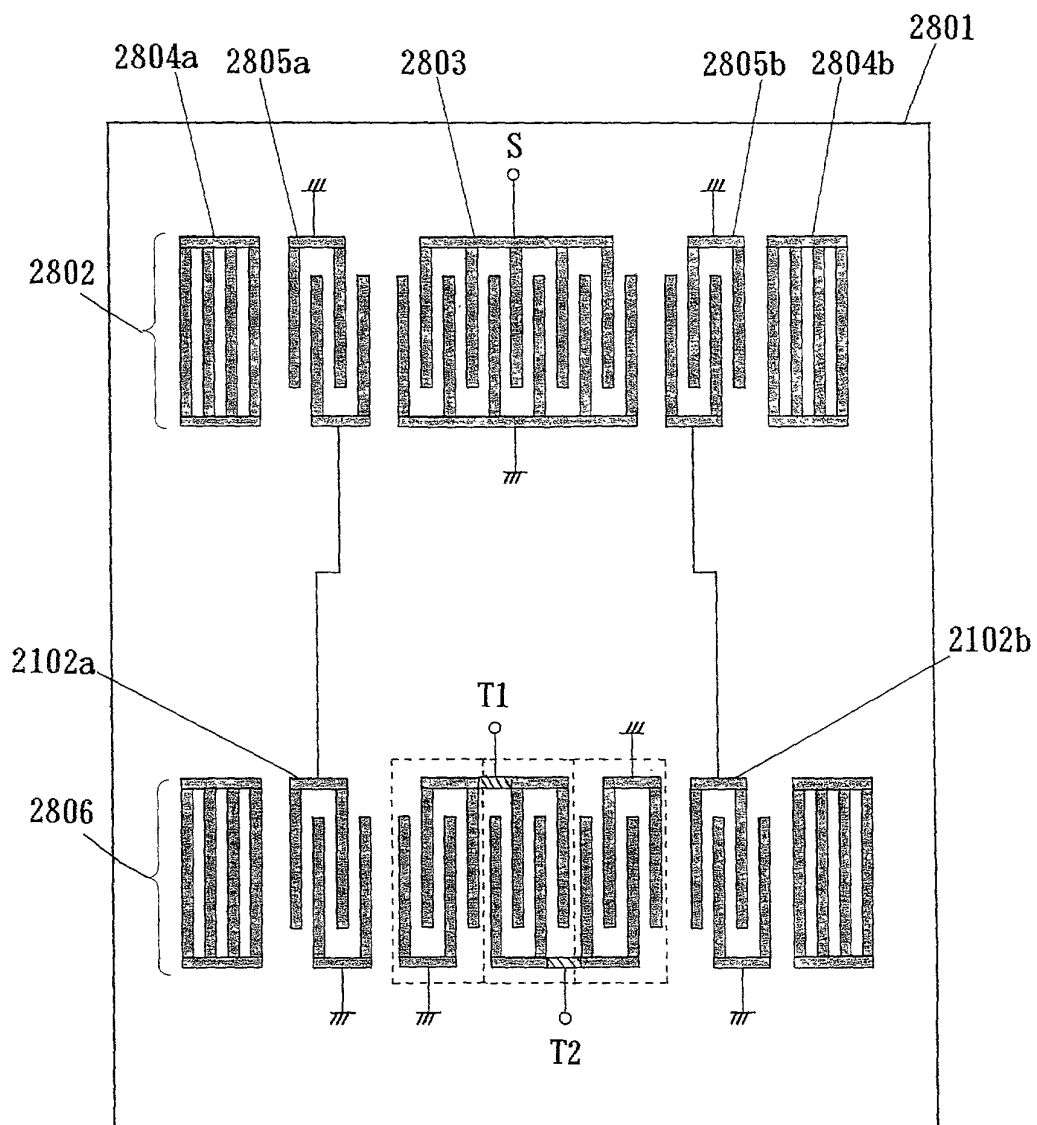


Fig. A9

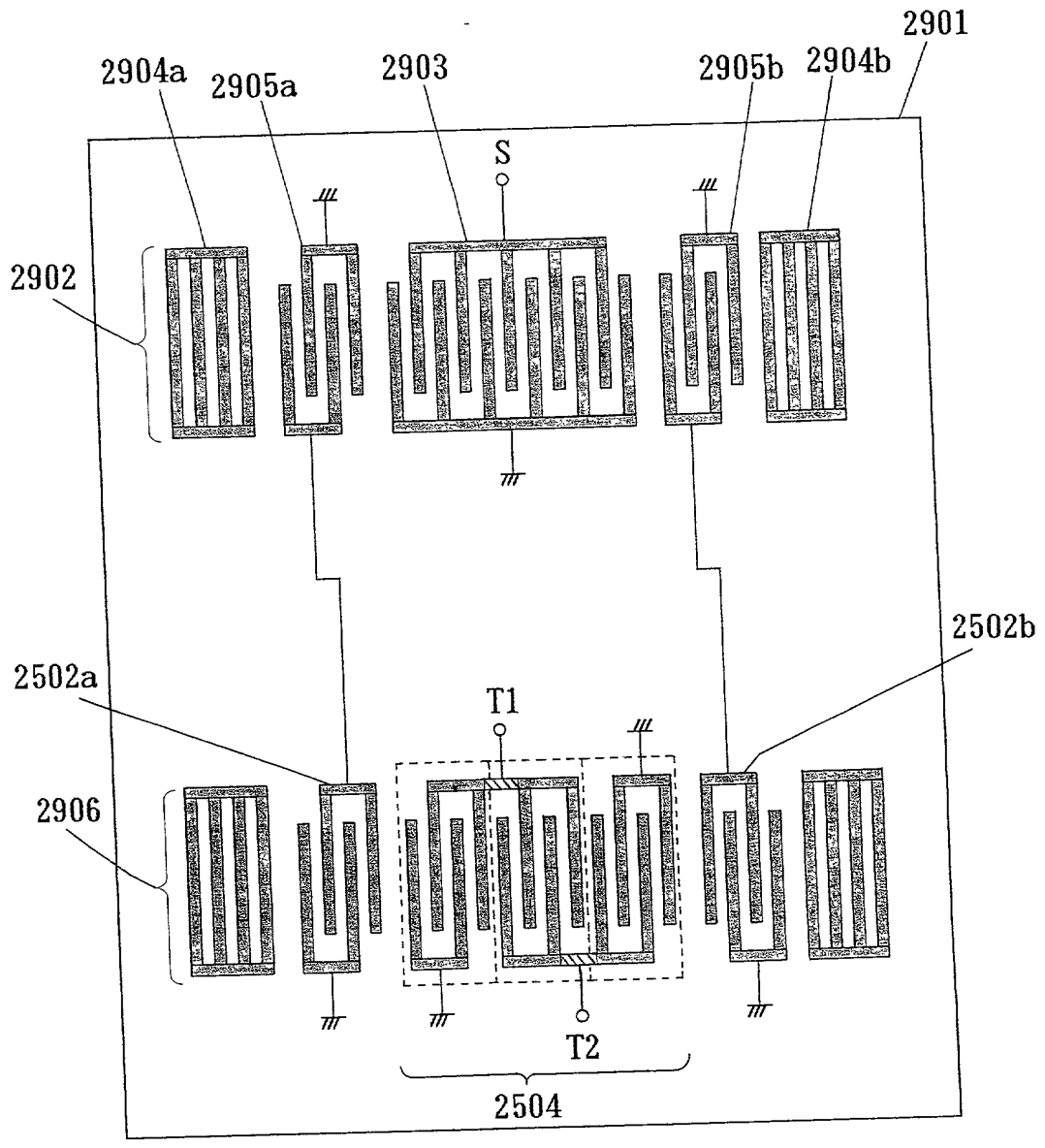


Fig. A10

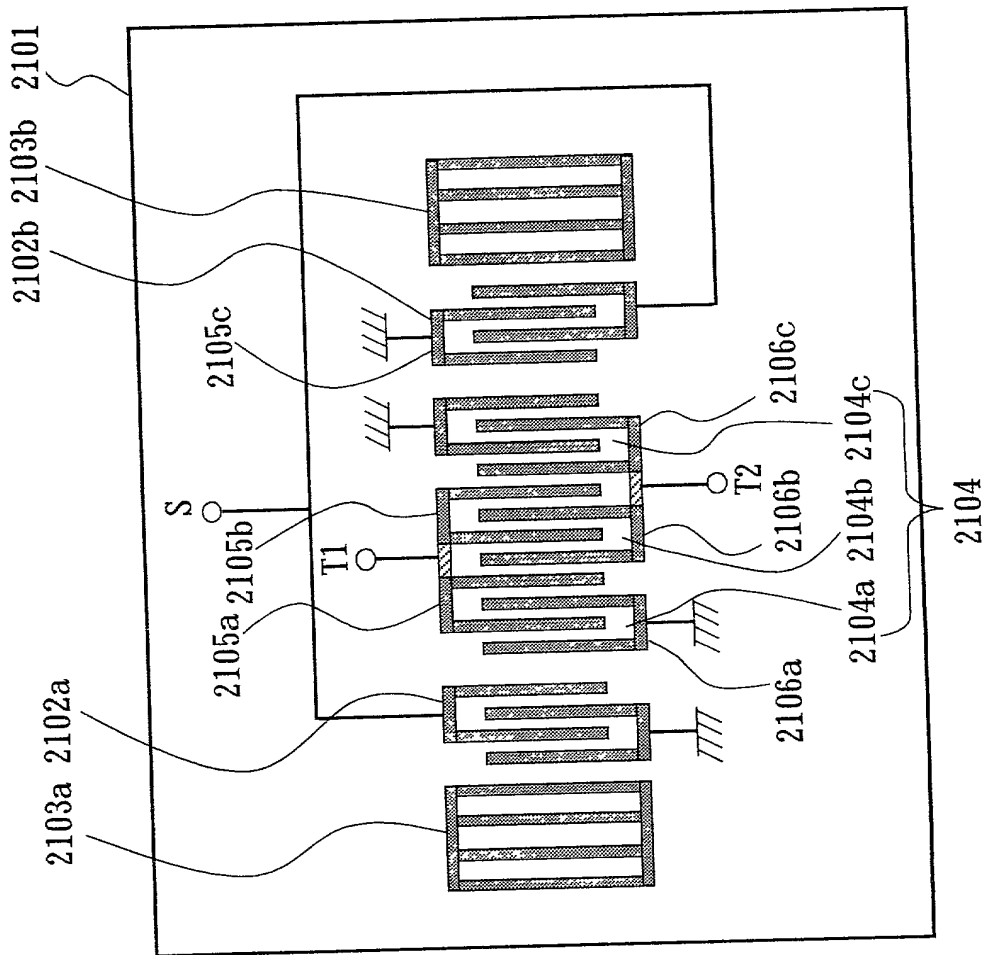


Fig. A11

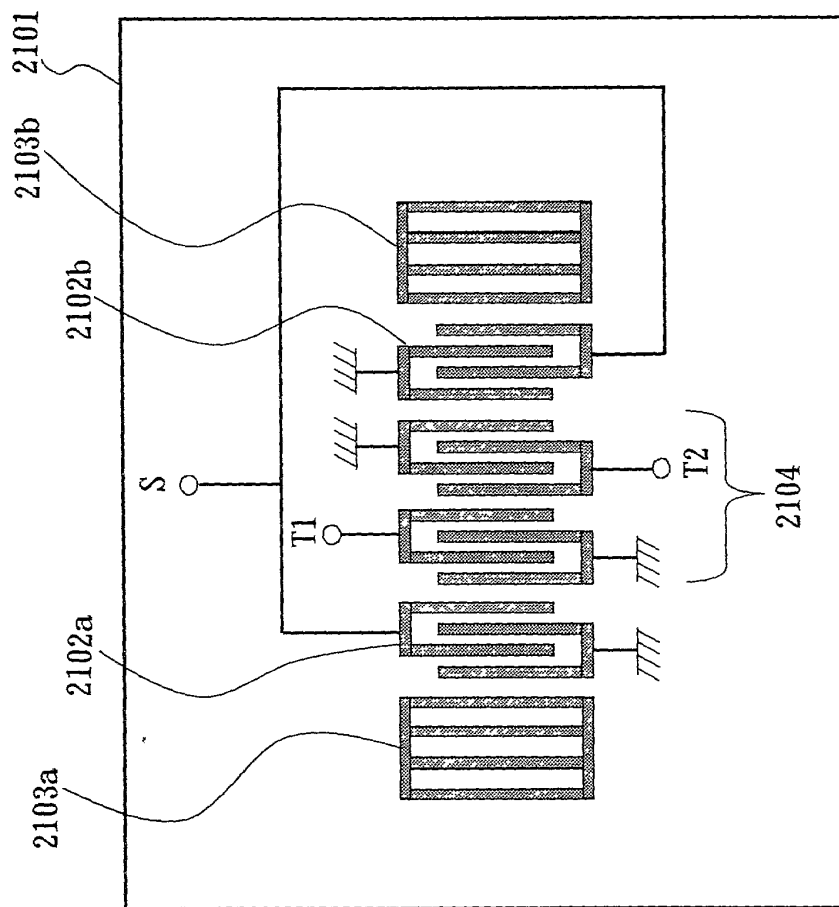


Fig. A12 PRIOR ART

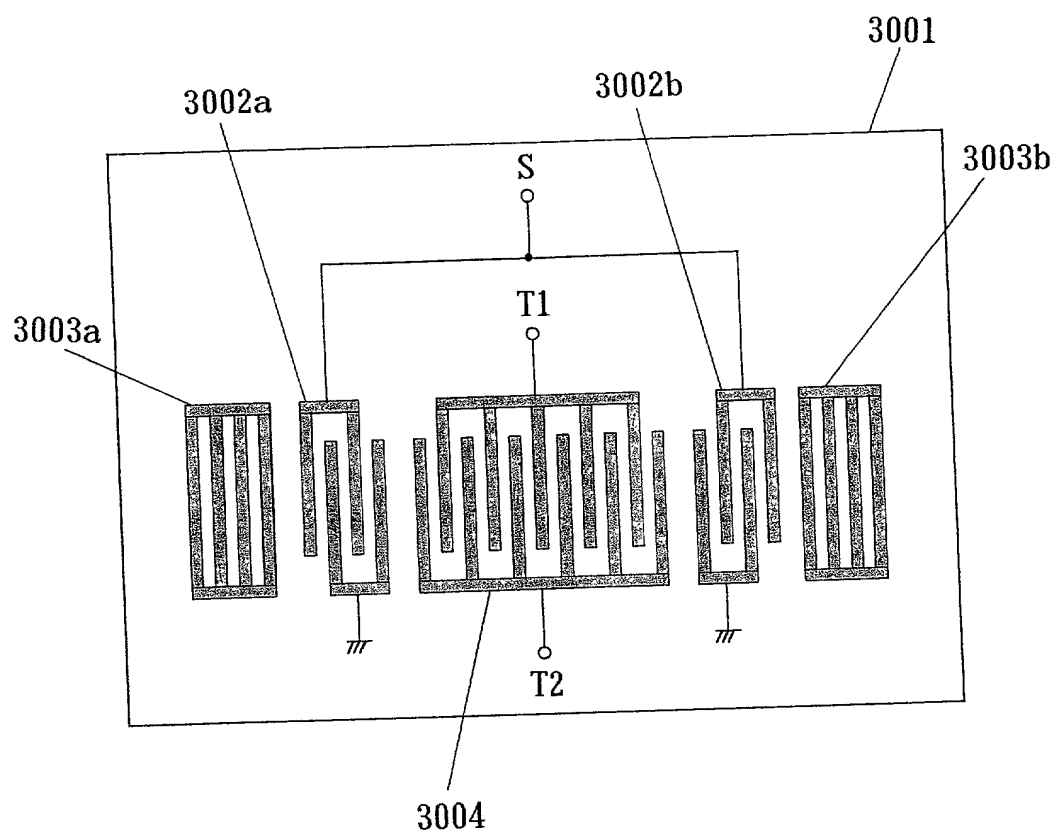


Fig. A13

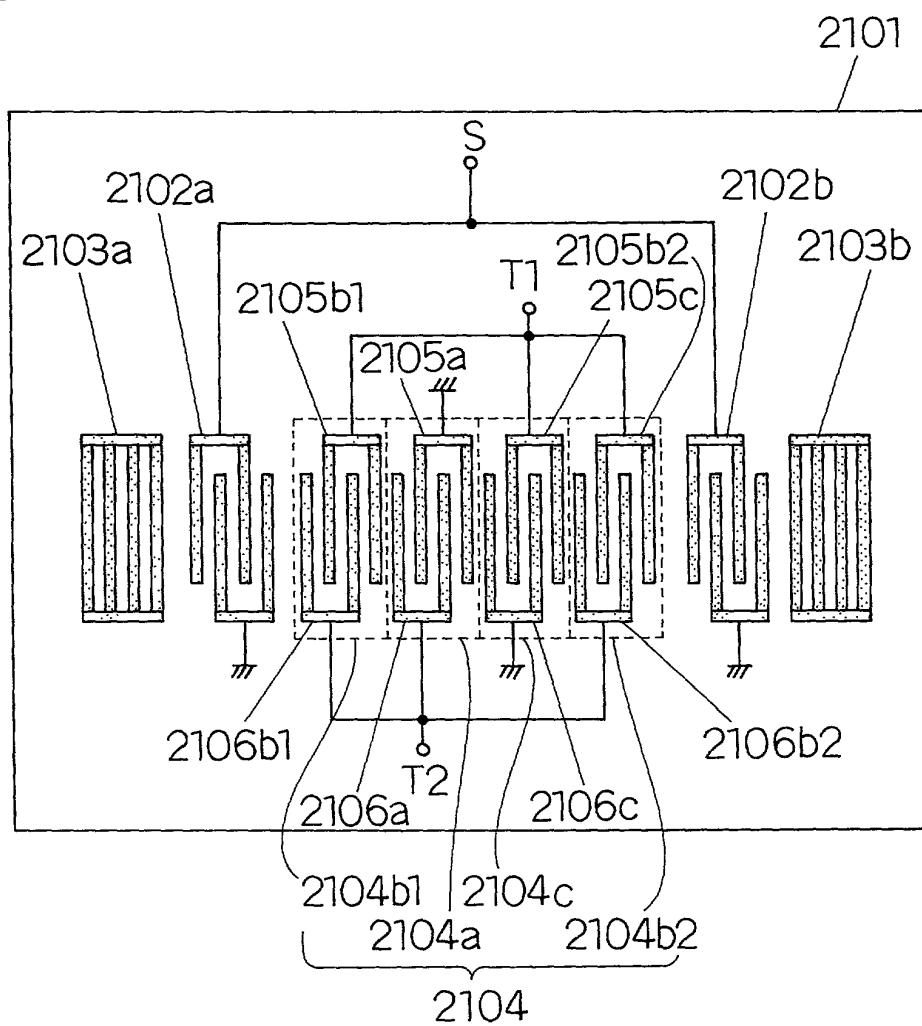


Fig. A14

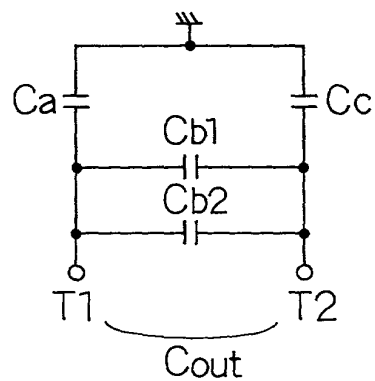


Fig. A15

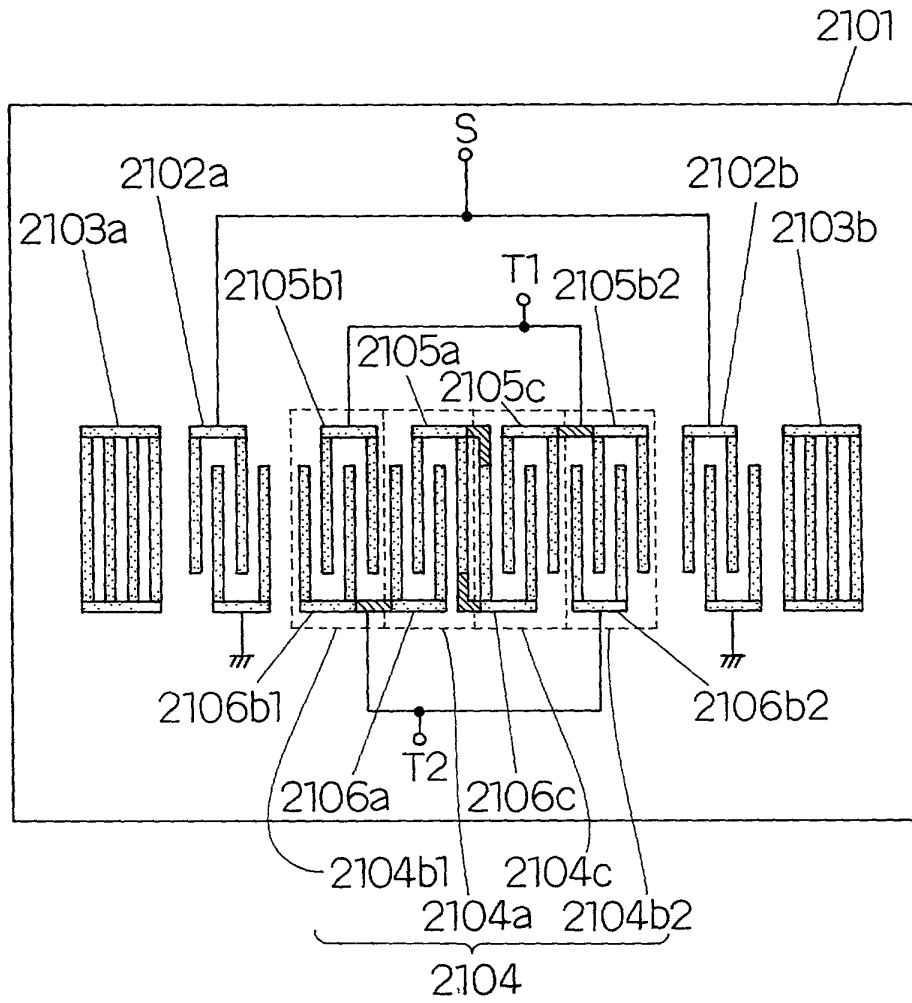


Fig. A16

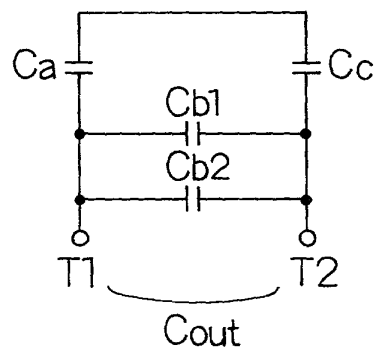




Fig. A17

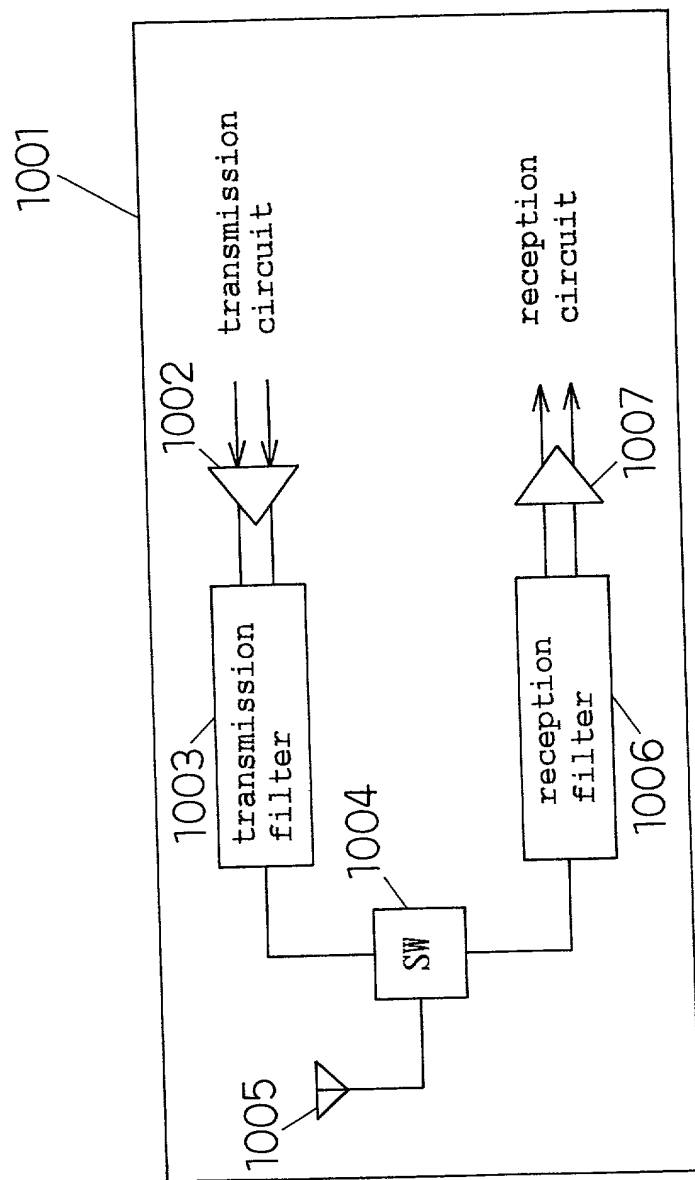




Fig. B2

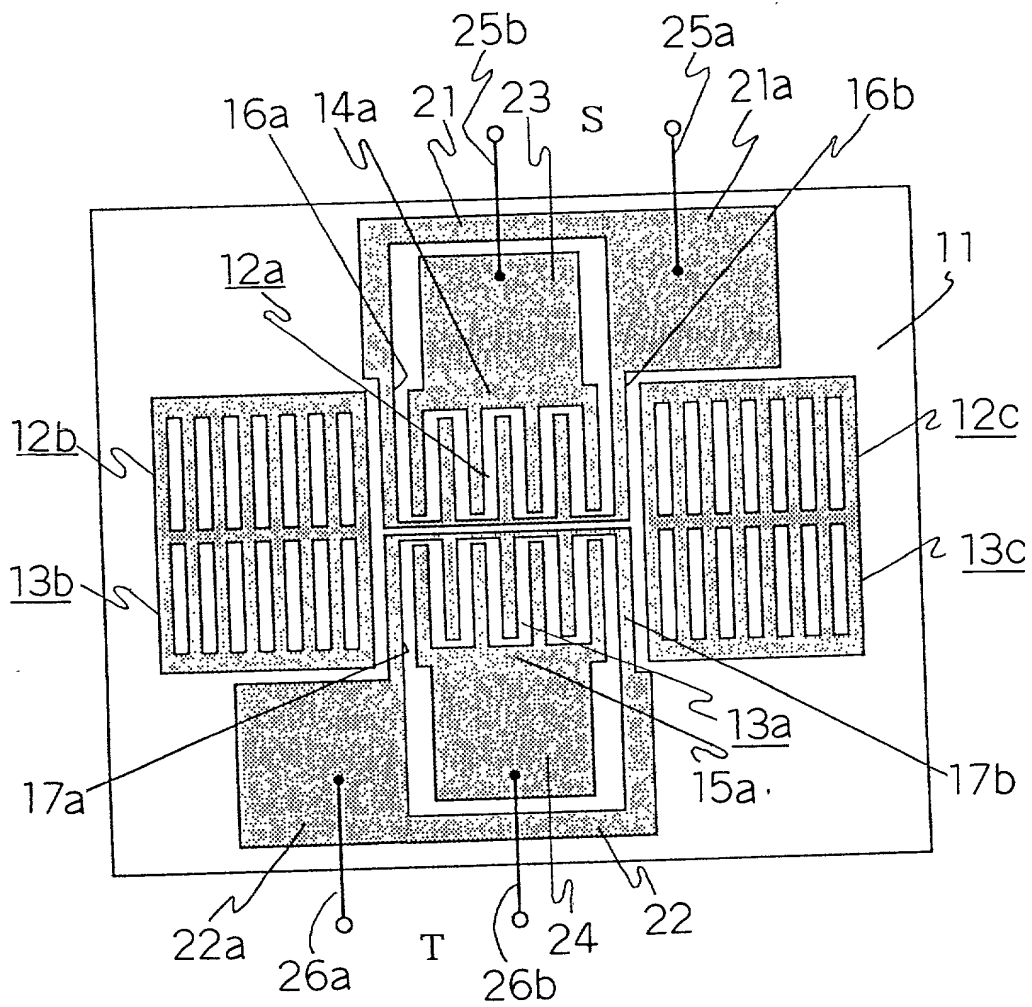
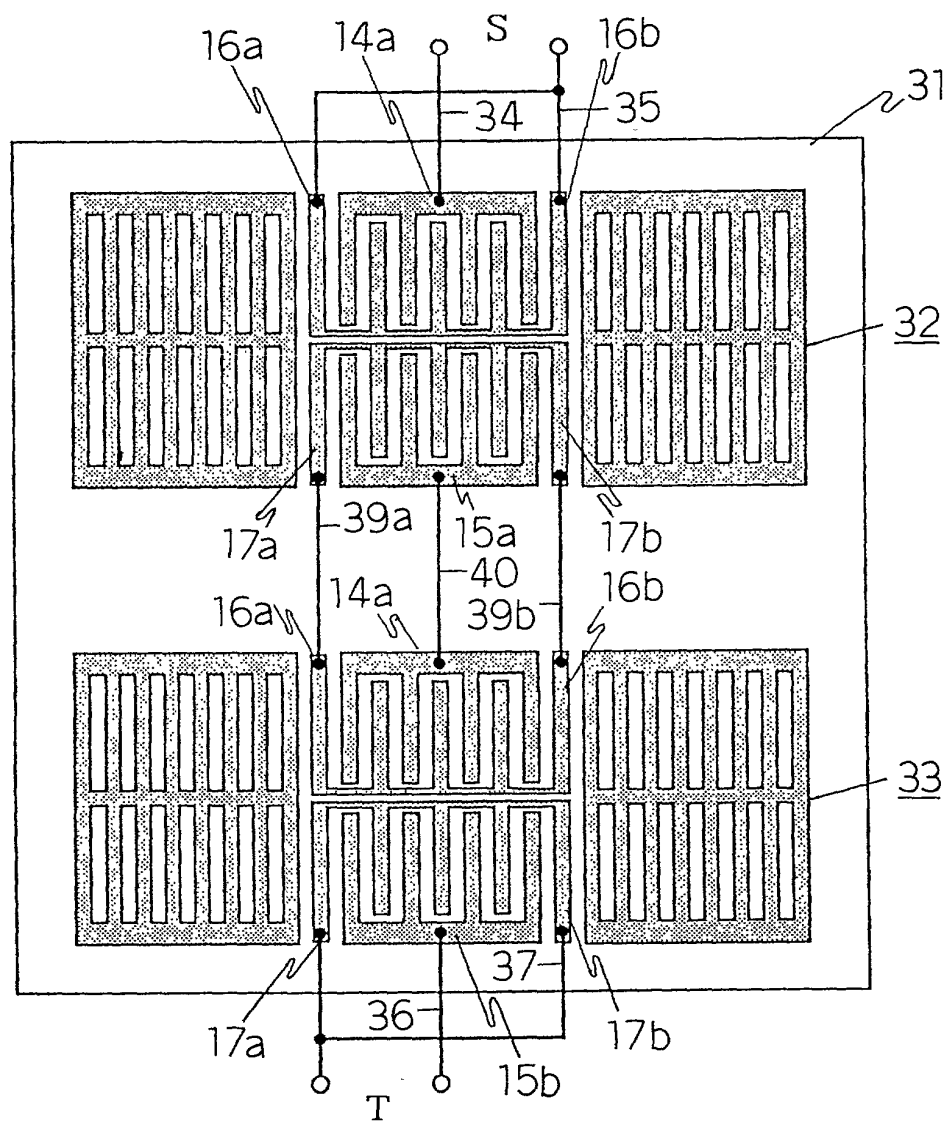
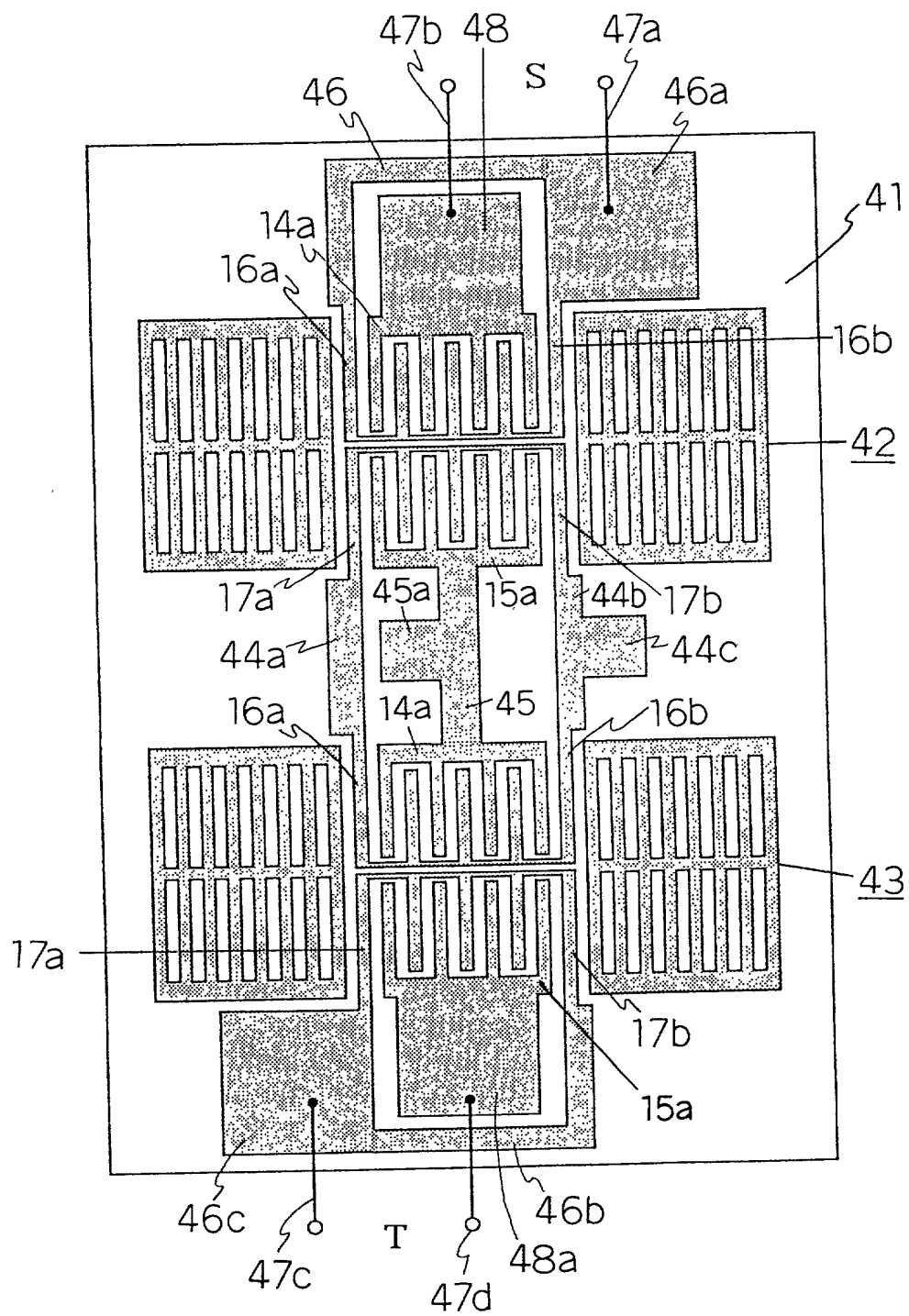


Fig. B3



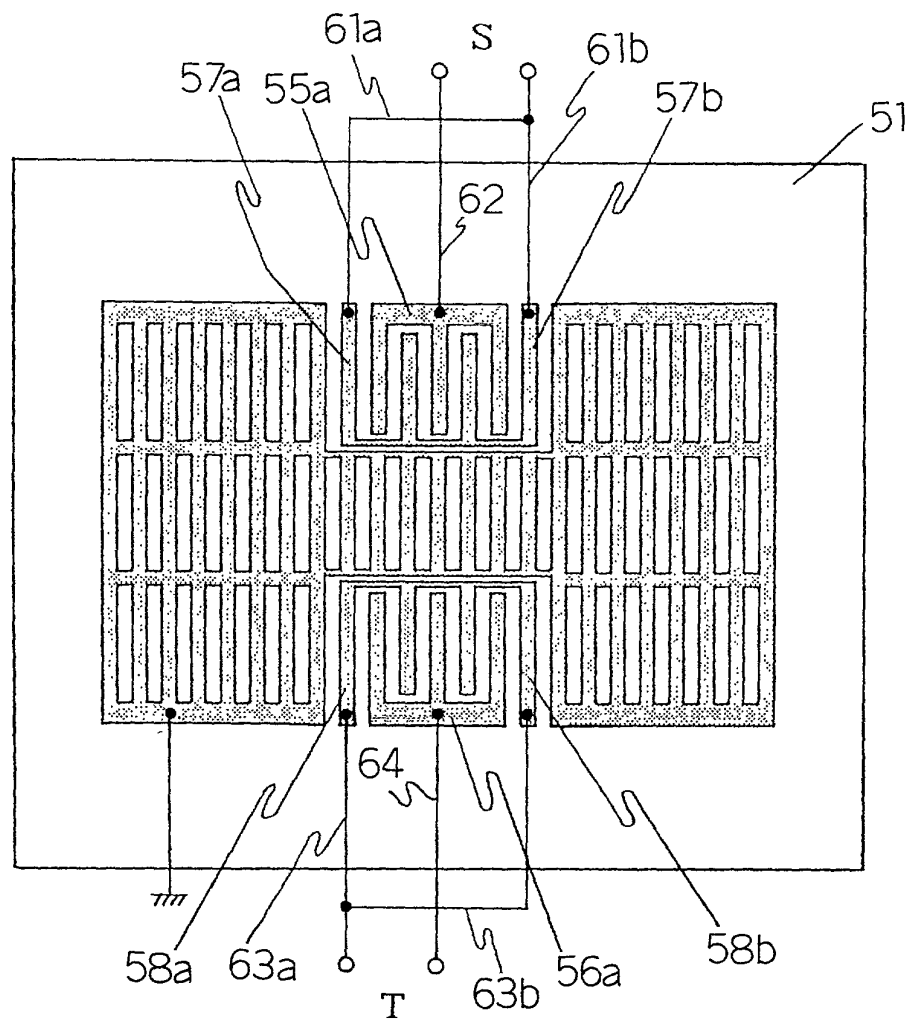
10051310-012202

Fig. B4



[illegible]

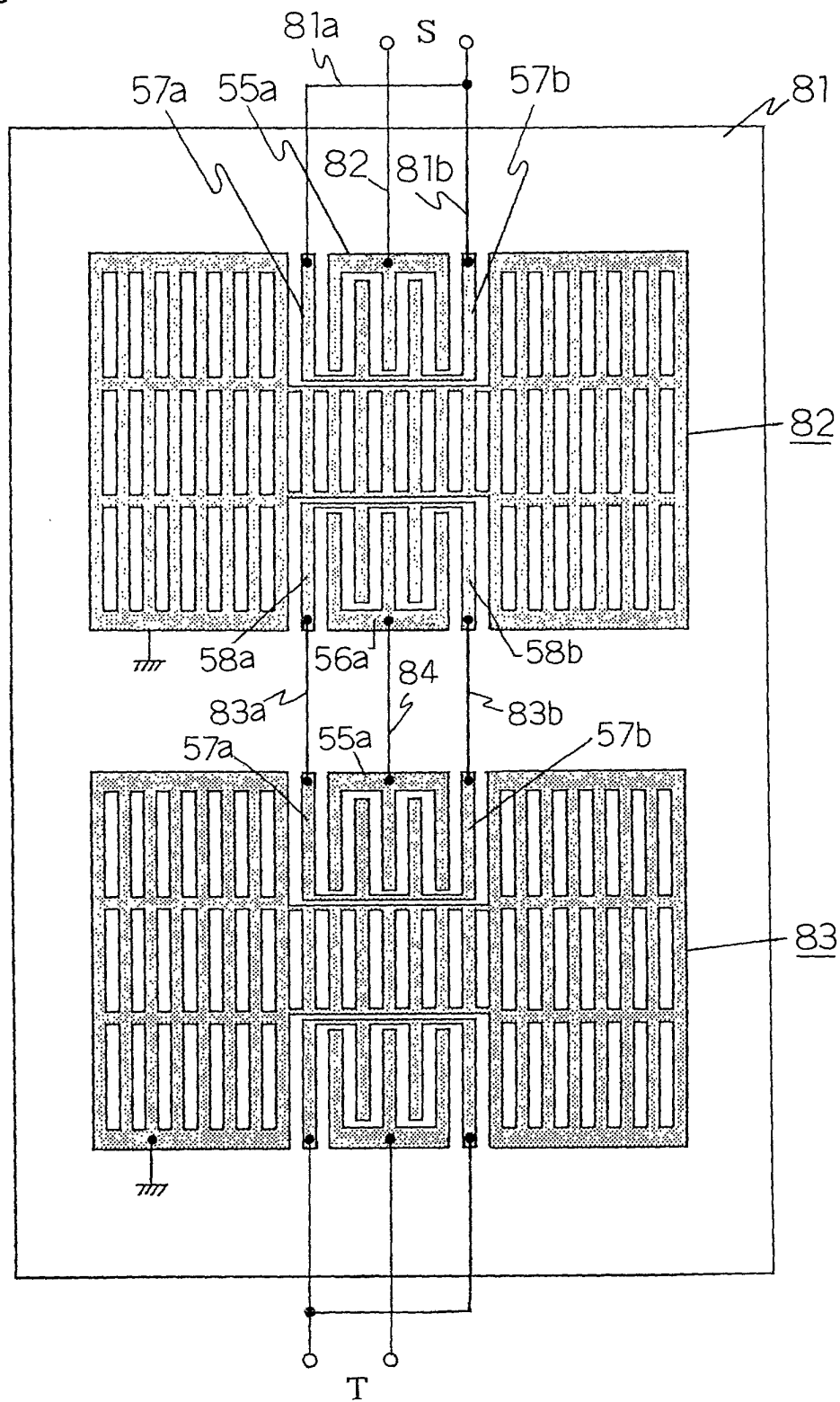
Fig. B6



[illegible]



Fig. B8



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Fig. B11 (b)

Fig. B11 (a)

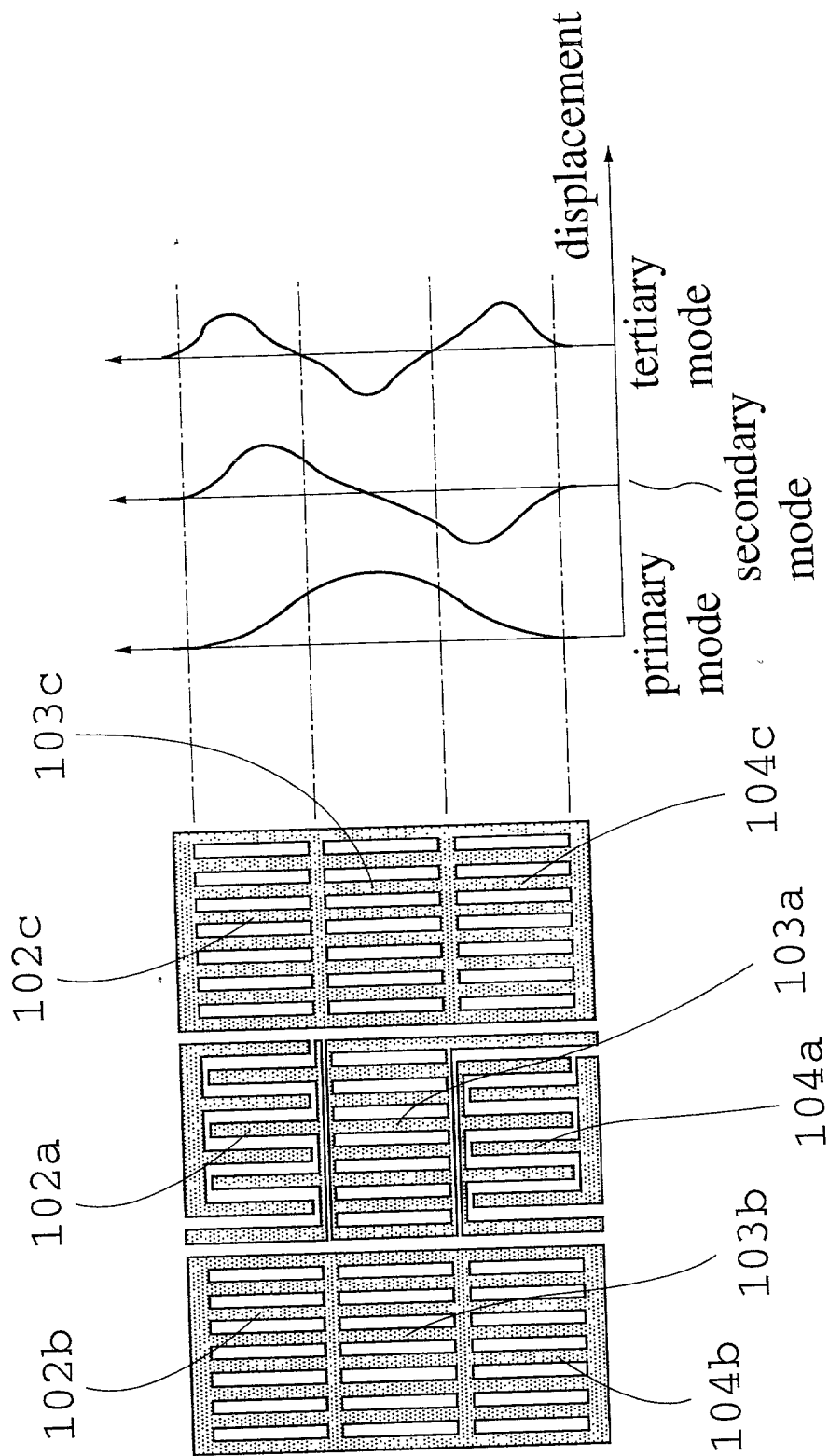


Fig. B12

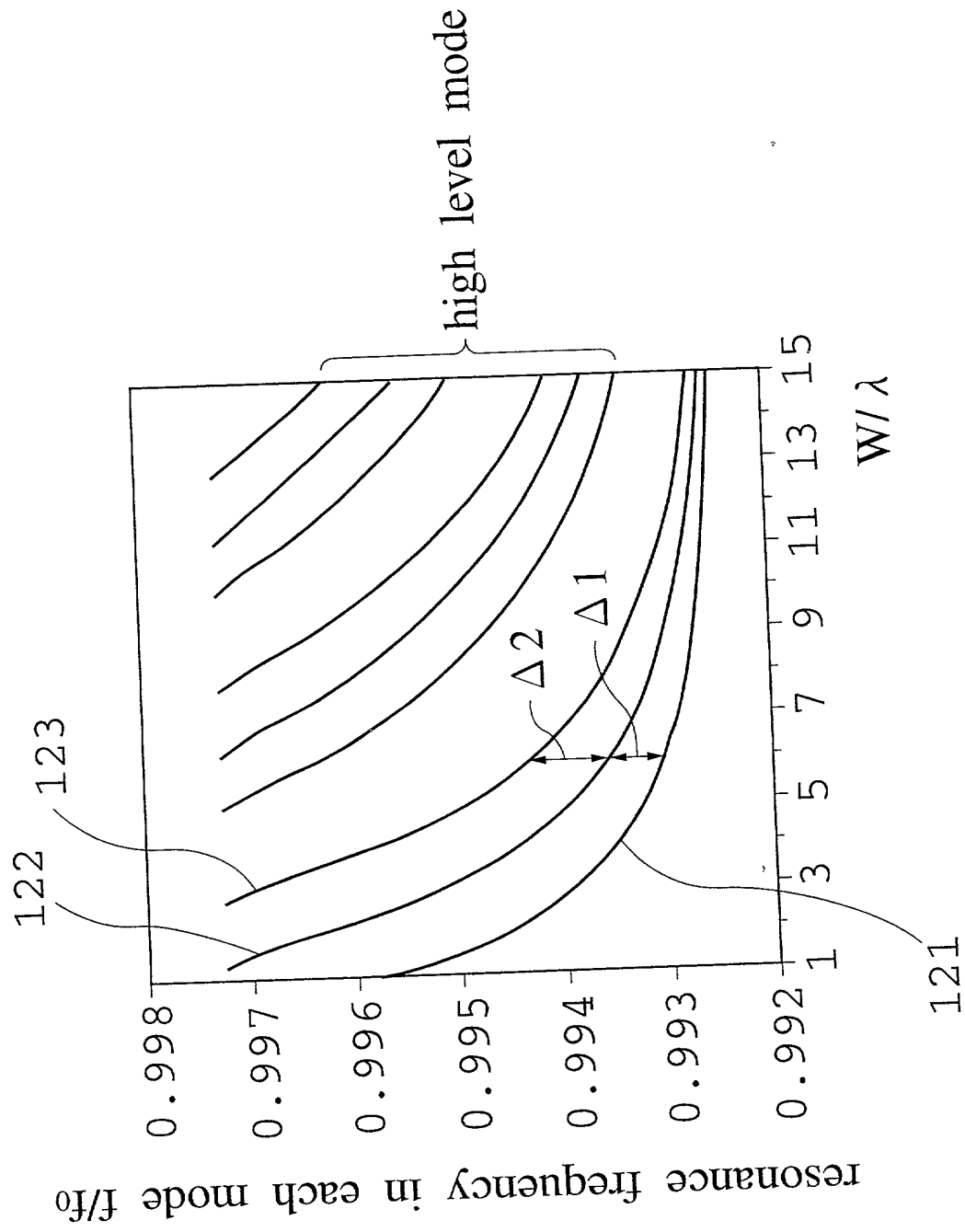


Fig. B13

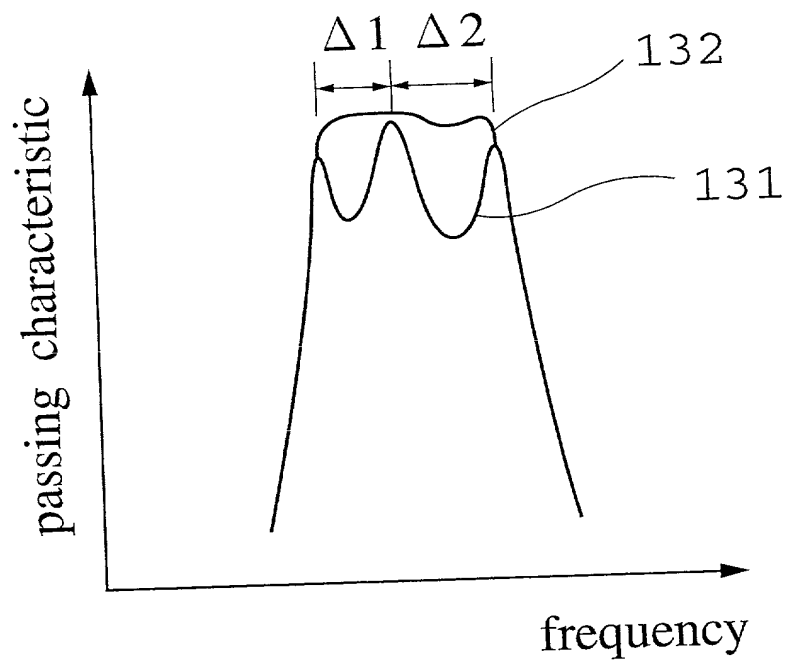


Fig. B14

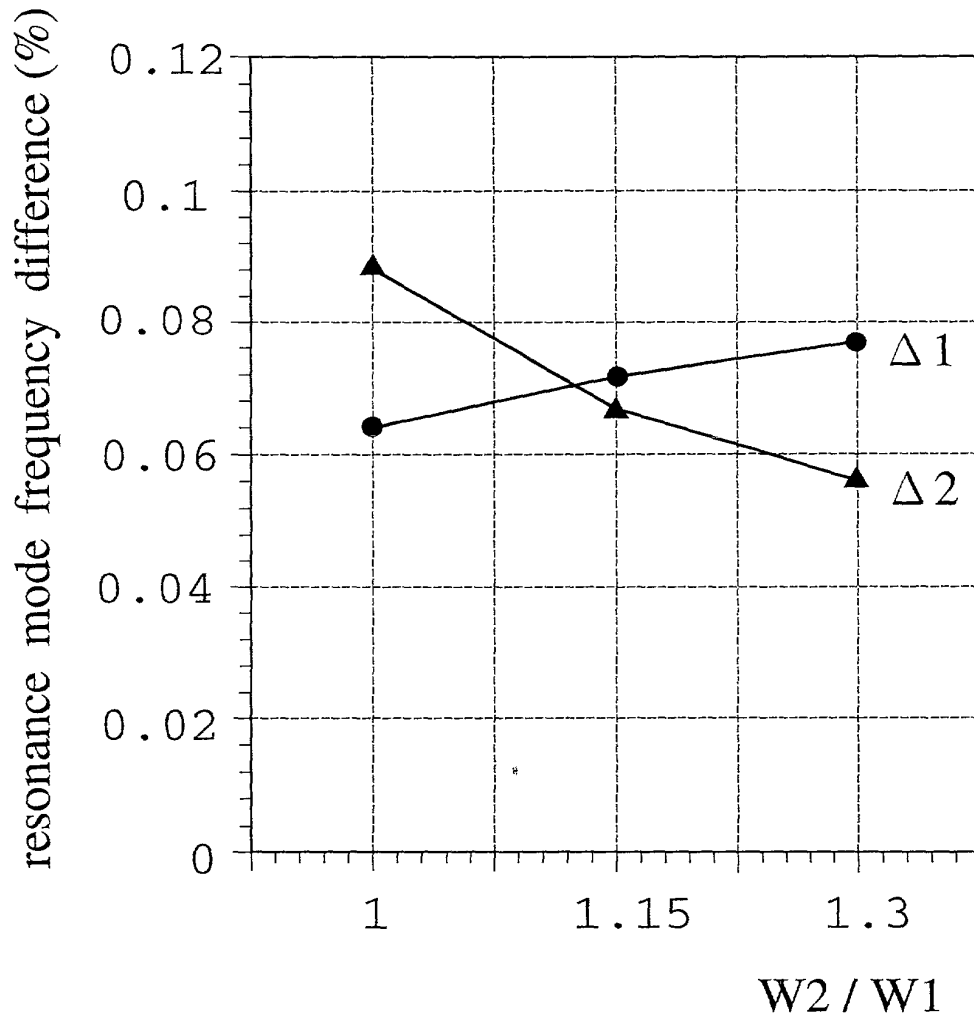


Fig. B15

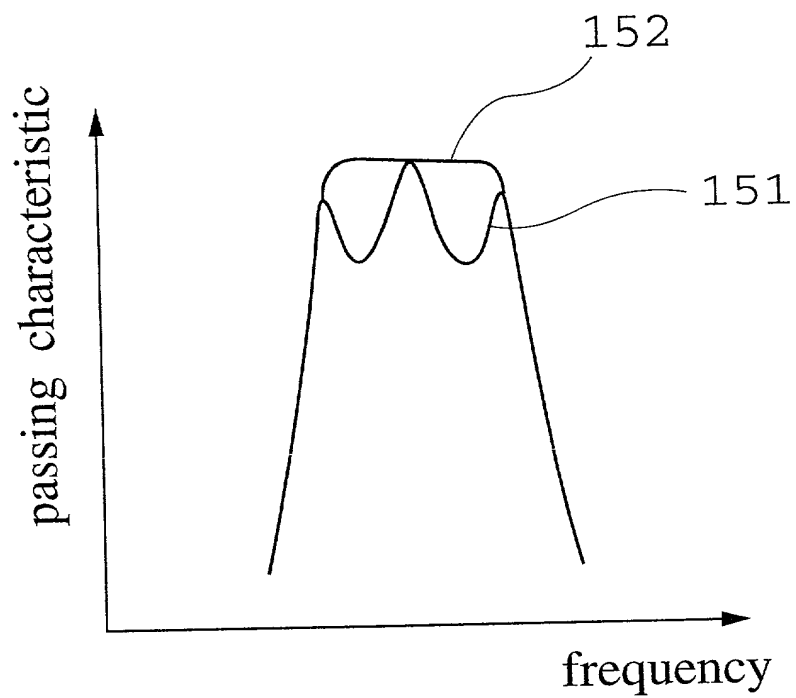




Fig. B16

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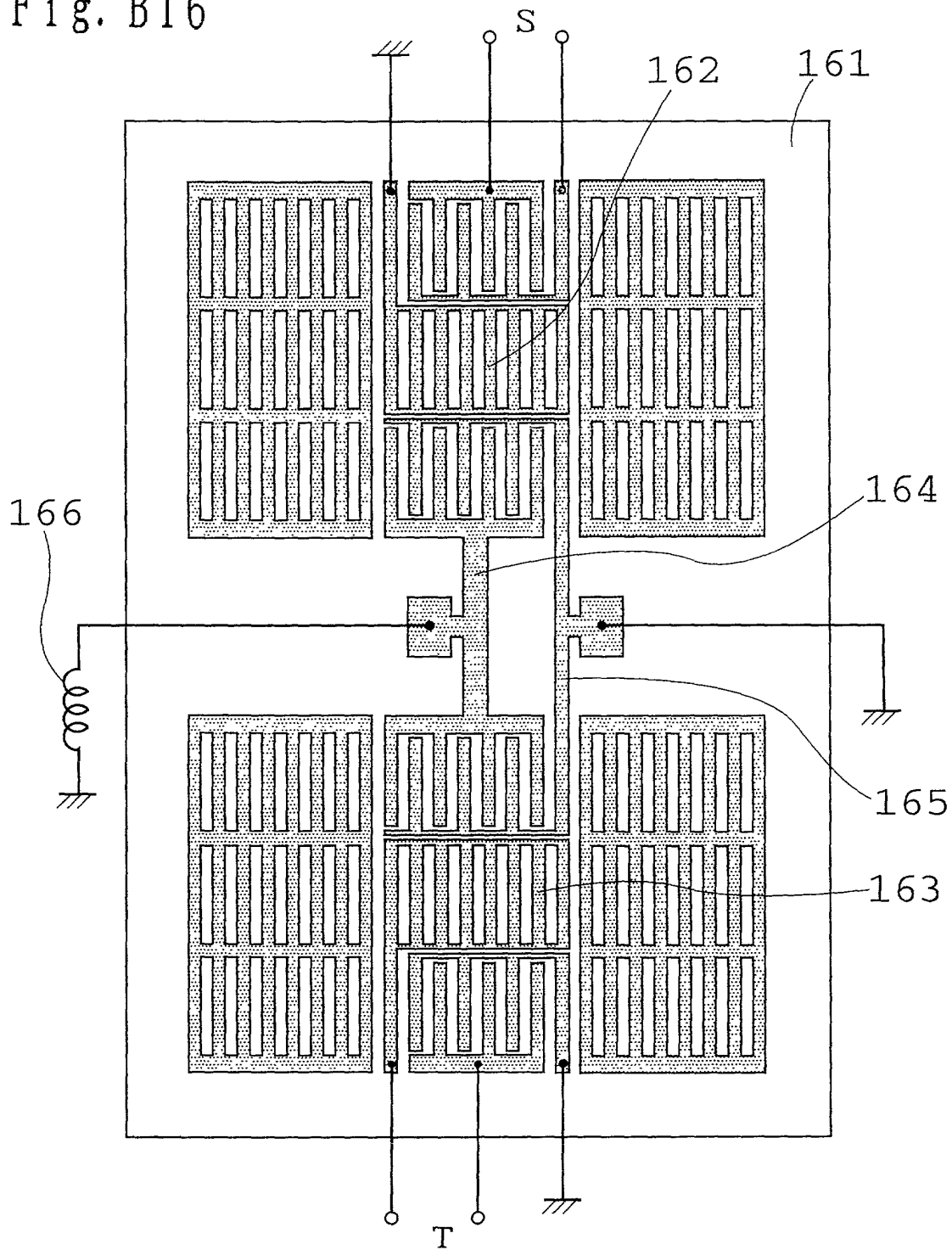


Fig. B17

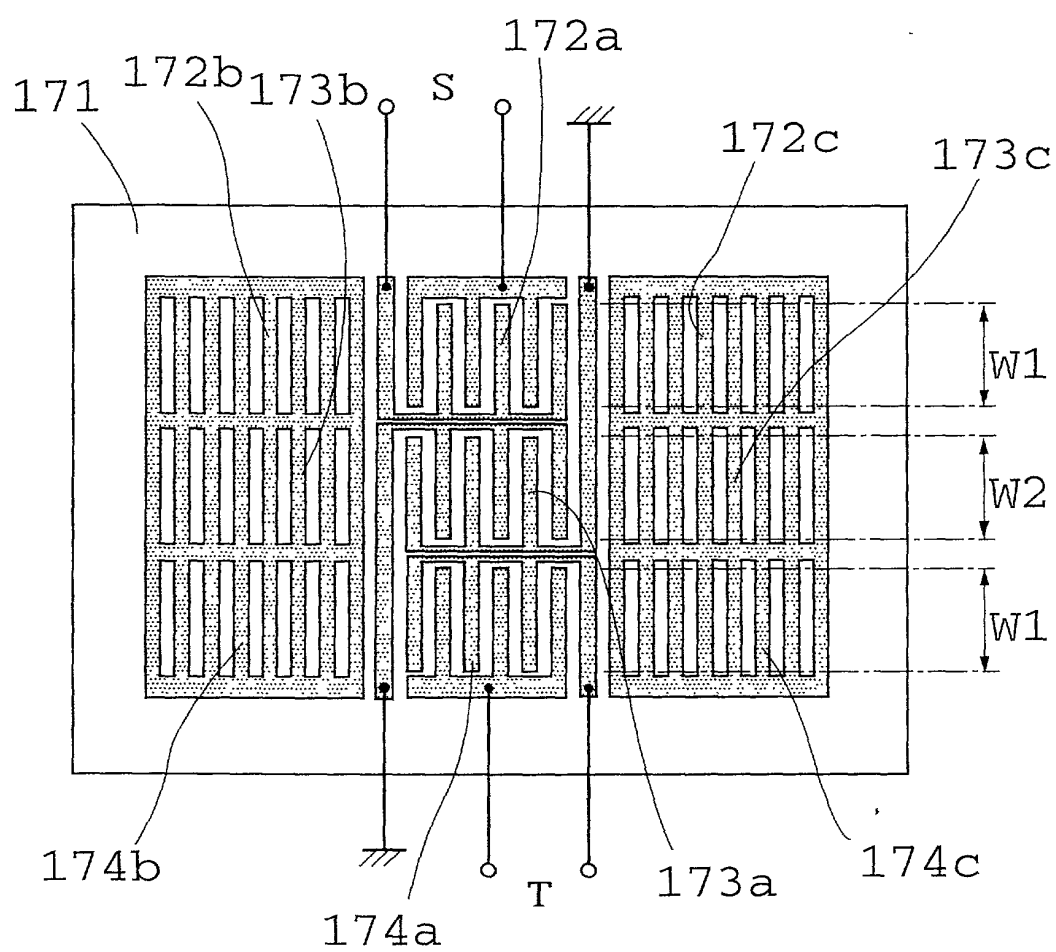




Fig. B19

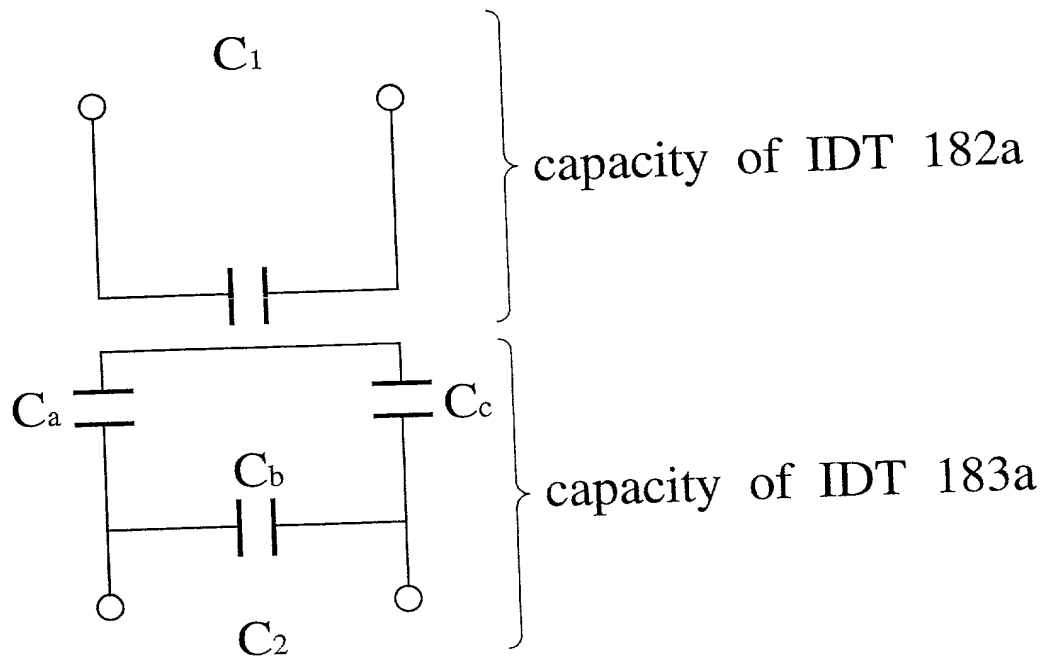
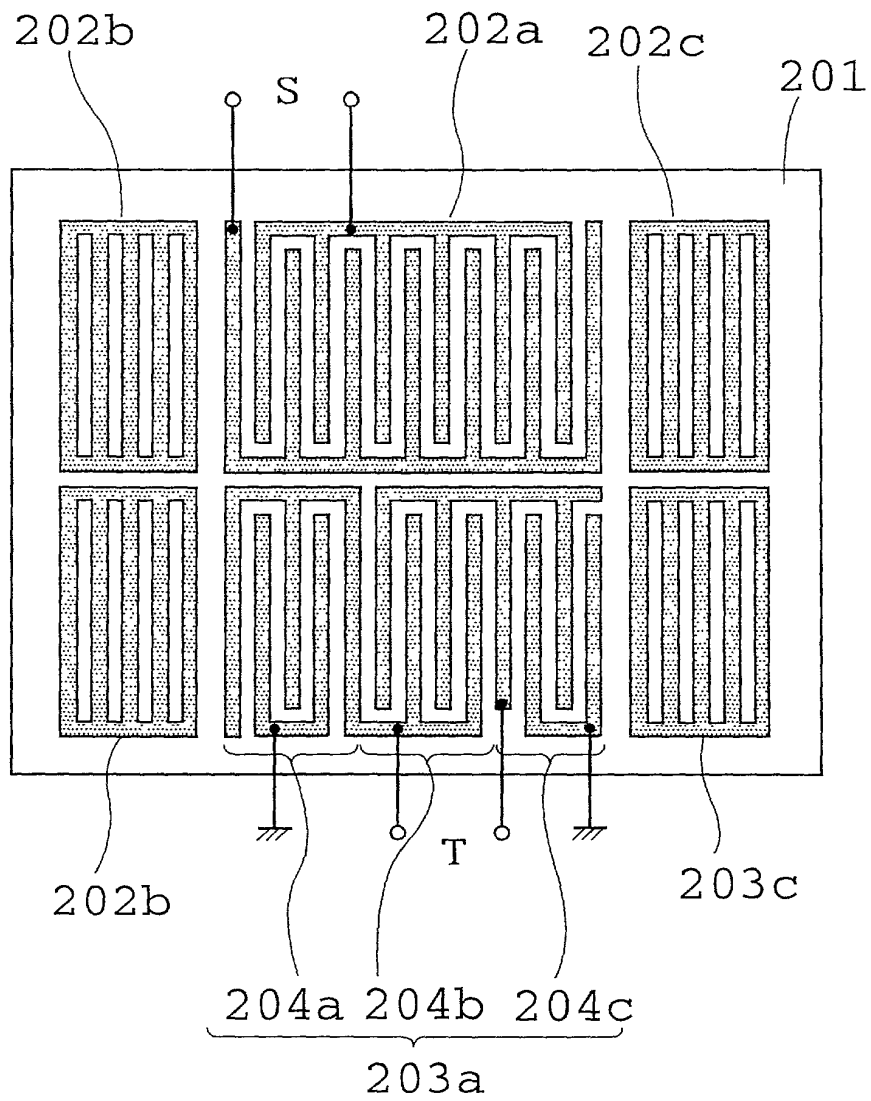
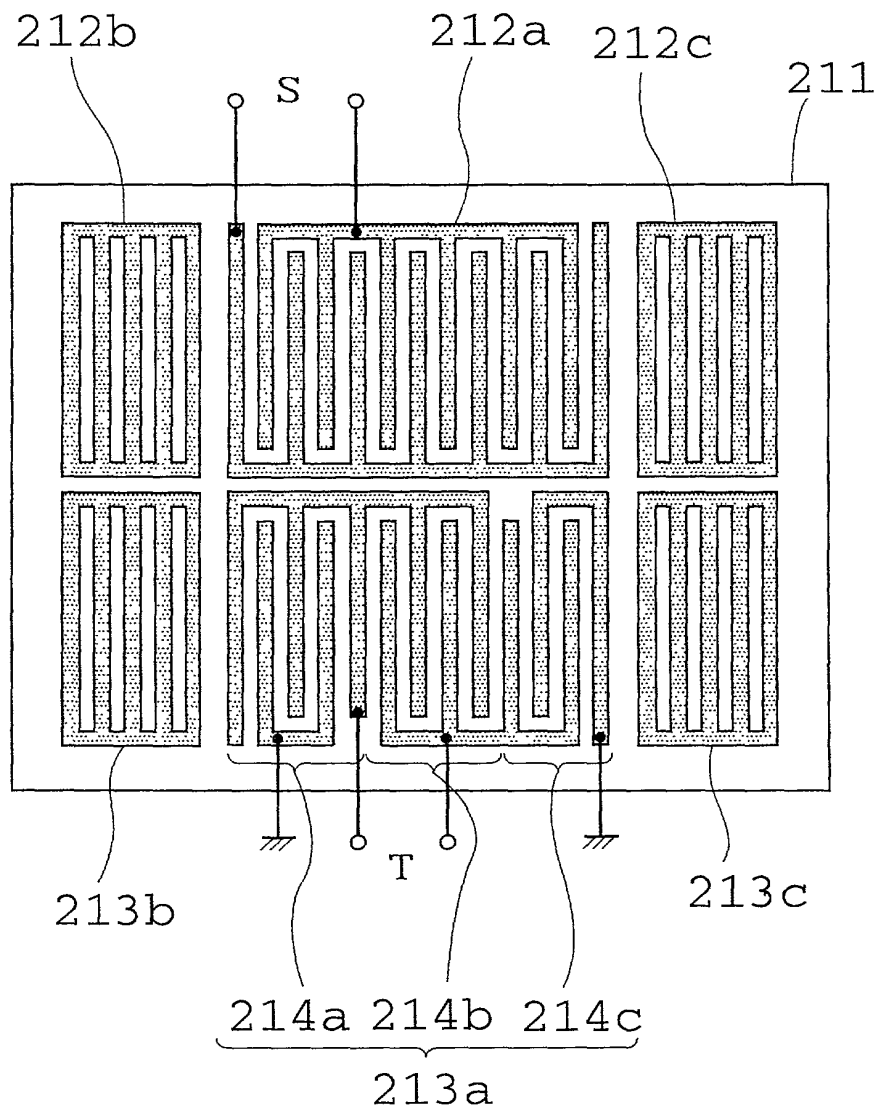


Fig. B20



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Fig. B21



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Fig. B22

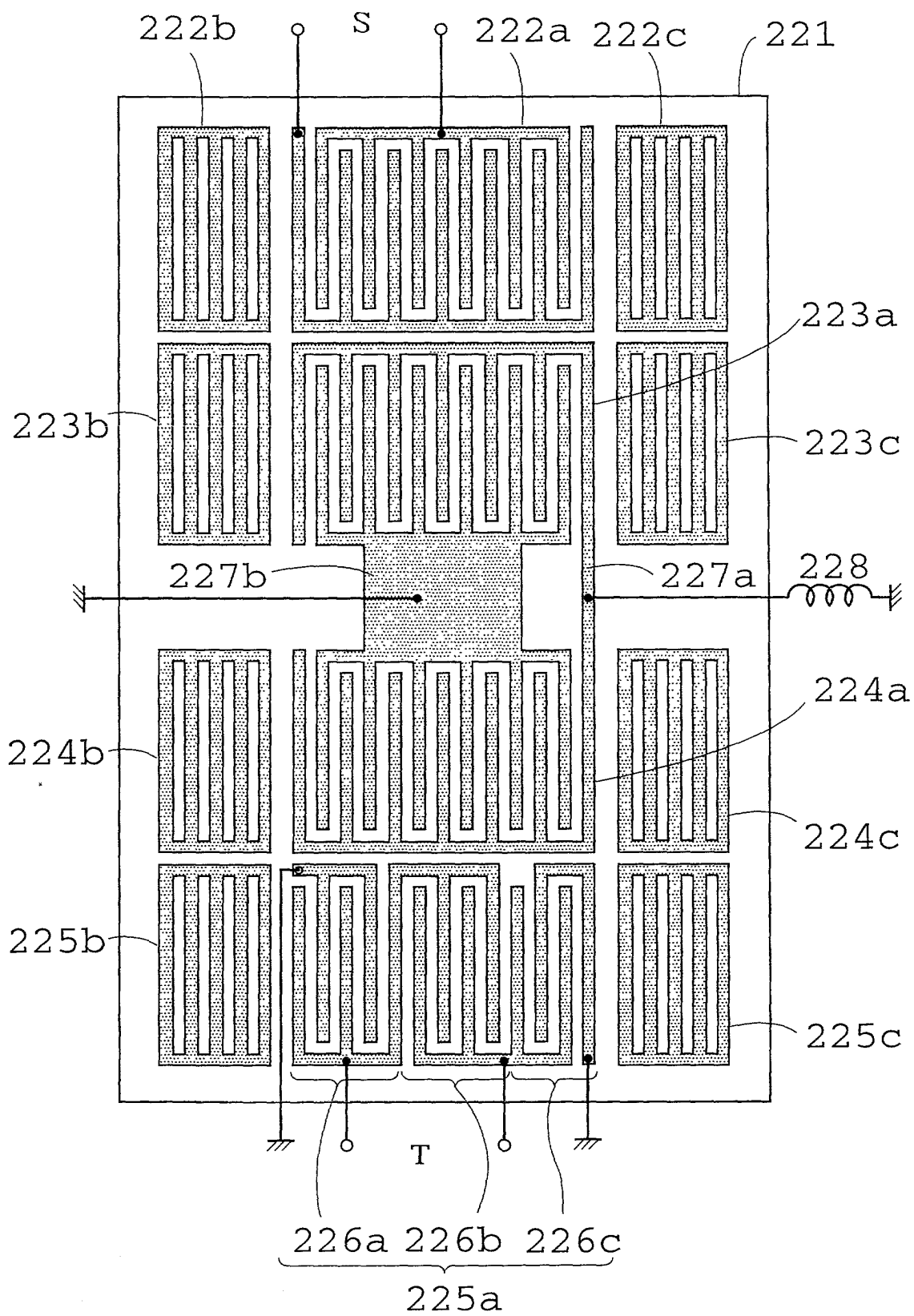
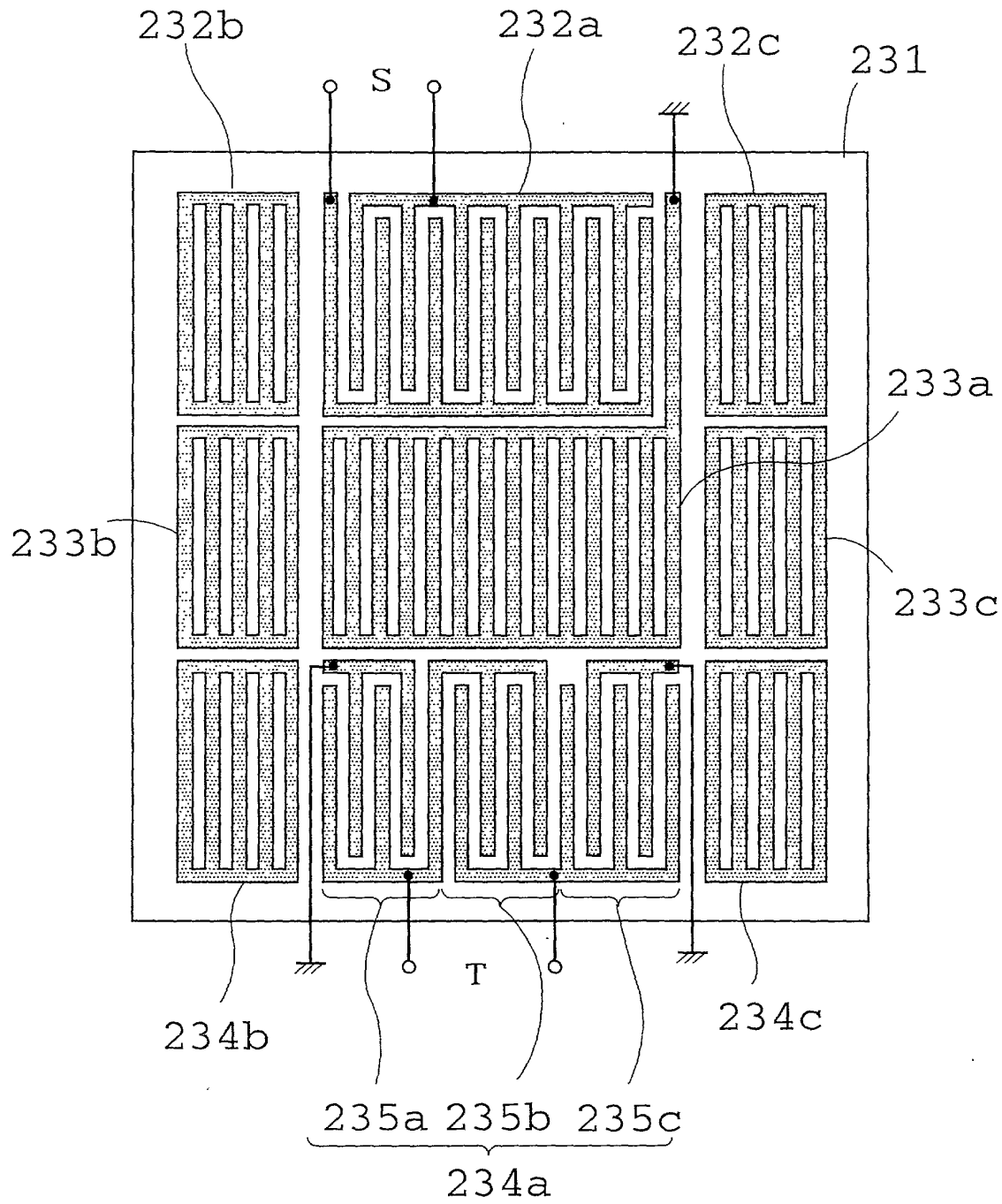


Fig. B23



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Fig. B24 PRIOR ART

